National University of Sciences & Technology (NUST)
School of Electrical Engineering and Computer Science (SEECS)
Department of Electrical Engineering

Digital Logic Design

Course Code:	CS-116	**Semester:**	Spring 2024
Credit Hours:	2+1	**Pre-requisites:**	Nil
Instructor:	Engr. Arshad Nazir	**E-mail:**	arshad.nazir@seecs.edu.pk
Office:	Room A-215, Faculty Block	**Telephone:**	+92 (0)51 9085 2117
Students Batch:	BSCS-13ABC	**Discipline/Year:**	Computer Science/First
Lecture/Lab Days:	**Mon:**1000-1050 (C/CR-04) **Tues:**1000-1050 (B/CR-03) 1100-1150 (A/CR-02) 1400-1650 (C/Digital Lab) **Wed:** 1200-1250 (C/CR-04) 1400-1450 (A/CR-02) 1500-1550 (B/CR-03) **Thu:** No class **Fri:** 1000-1250 (A/Digital Lab) 1400-1650 (B/Digital Lab)	**Consulting Hours:**	**Tues:** 1200-1300 Hrs.(A/Office) **Wed:** 1600-1650 Hrs.(B/Office) **Mon:** 1200-1300 Hrs.(C/Office) or via email/WhatsApp
Lab Engr Sec AB:	Engr. Abdul Rahman	**E-mail:**	Abdul.rahman1@seecs.edu.pk
Lab Engr Sec C:	Engr. Mughees Ahmed	**E-mail:**	mughees.ahmed@seecs.edu.pk
Knowledge Group:	Digital Systems and Signal Processing	**Updates on LMS:**	on required basis

Course Description:

Digital Logic Design is a one-semester course taken by Computer Science students during first year of their engineering program. This course introduces the logic operators and gates to lay the framework for strengthening the basic understanding of computer building blocks. Both combinational and sequential circuits are studied in this course along with their constituent elements comprising Arithmetic circuits, Comparators, Decoders, Encoders, Multiplexers, Tri-state gates as well as Latches, Flip-flops, Counters and Registers. It lays down foundations for advanced studies in Computer Architecture & Organization (CAO), and Computer Organization and Assembly Language (COAL) Systems to be taught in the following semester.

Course Objectives:

In this course students will learn principles of Digital Logic Design. They will combine classical design methodologies with a series of laboratory assignments in which they will demonstrate their ability to successfully design, implement, and debug digital systems using Computer Aided Design tools and physical prototyping.

Course Learning Outcomes (CLO)

Upon successful completion of this course the students will be able to demonstrate the following: -		**BT LEVEL**	**PLO**
1	**Understand** the Digital principles, arithmetic operations, and different simplification techniques required to model any computing system.	C2	1
2	**Apply** the acquired knowledge towards logic circuits optimization in a computing system.	C3	2
3	**Analyze** combinational and sequential circuits forming key ingredient of any	C4	3

	computing system.		
4	**Design** combinational and sequential circuits of moderate complexity within given hardware constraints.	C5	4
5	**Construct** digital systems of moderate complexity using laboratory equipment and simulation tools.	P4	5
6	**Function** effectively both individually and as a member of a team	A4	6
7	**Exhibit** good professional and ethical behavior**. Adhere** to lab safety rules.	A5	9
* BT=Bloom's Taxonomy, C=Cognitive domain, P=Psychomotor domain, A=Affective domain			

Mapping of CLOs TO Program Learning Outcomes

PLOs/ CLOs	CLO-1	CLO-2	CLO-3	CLO-4	CLO-5	CLO-6	CLO-7
PLO1 (Academic Education)	√						
PLO2 (Knowledge for solving Computing problems)		√					
PLO3 (Problem Analysis)			√				
PLO4 (Design/Development of solutions)				√			
PLO5 (Modern tool usage)					√		
PLO6 (Individual and Teamwork)						√	
PLO7 (Communications)							
PLO8 (Computing Professionalism and Society)							
PLO9 (Ethics)							√
PLO10 (Life-long Learning)							

Mapping of CLOs to Assessment Modules and Weight ages (in accordance with NUST statutes)

To be filled in at the end of the course

CLOs\PLOs	CLO-1	CLO-2	CLO-3	CLO-4	CLO-5	CLO-65	CLO-7
Quizzes: 15% (**10**)	√	√	√				
Assignments: 6% (**4**)	√	√	√				
Mid Semester Exam: 30% (**20**)	√	√	√				
Labs: 70% **(23)**				√	√	√	√
Project: 30% (10)				√	√	√	√
End Semester Exam: 50% (**33**)	√	√	√				
Total: 100							

Books:

Text Book: Digital Design (Fourth Edition) by M. Morris Mano and Michael Ciletti

Reference Books:

1. Digital Fundamentals (Eleventh Edition) by Floyd
2. Logic and Computer Design Fundamentals (Fourth Edition) by M. Morris Mano and Charles R. Kime
3. Fundamentals of Logic Design (Sixth Edition) by Charles H. Roth Jr
4. Digital Systems: Principles and Applications (Tenth Edition) by TocciWidmer

5. Contemporary Logic Design (Second Edition) by Randy H. Katz
6. Verilog HDL: A guide to Digital Design and Synthesis (Second Edition) by Samir Palnitkar

Main Topics to be Covered:

1. Digital Systems. Binary Numbers. Number Base Conversions. Octal and Hexadecimal Numbers. Complements. Signed Numbers. Binary Codes.
2. Basic Definitions. Axiomatic Definition of Boolean algebra. Basic Theorems and Properties of Boolean Algebra
3. Boolean Functions. Canonical and Standard Forms. Other Logic Operations. Digital Logic Gates. Integrated Circuits
4. The K-Map Method. Four-Variable Map. Product of Sums and Sum of Products simplifications. Introduction to Five-Variable Map. Quine-McCluskey minimization technique (Tabulation).
5. Don't-Care Conditions. NAND and NOR Implementation. Other Two-Level Implementations
6. Combinational Circuits. Analysis Procedure. Design Procedure. Binary Adder-Subtractor. Decimal Adder. ALU Design using Combinational Circuits.
7. Binary Multiplier. Magnitude Comparator. Decoders. Encoders. Multiplexers
8. Sequential Circuits. Latches and Flip-flops
9. Analysis of Clocked Sequential Circuits.
10. Mealy and Moore FSM. State Reduction and Assignment. Design of clocked sequential circuits.
11. Registers. Shift Registers. Ripple Counters
12. Synchronous Counters. Other Counters

Lecture Breakdown:

Week No	Lecture	Topics	Text Book Reference	Other References	Remarks
1.	**1.**	**Introduction**: Digital Systems and motivation for study. Number Systems: Binary, Octal, Decimal and Hexadecimal Numbers and Base Conversions.	1-1, 1-2,1-3, &1-4	1-2 Ref Book (3)	
	2.	Complements: Subtraction of Unsigned Numbers using Complements.	1-5	.	
	Lab 01	Familiarization of Basic Gates and Digital ICs			
2.	3.	Signed Binary Numbers Arithmetic: Addition and Subtraction of Signed Binary Numbers.	1-6	2-6 Ref Book (2)	
	4.	Binary Codes. Binary Storage and Registers. Binary Logic: Definition of Binary Logic and Logic gates.	1-7, 1-8, & 1-9		
	Lab 02	Introduction to Verilog HDL. Basic language constructs and design entry			

		using Verilog HDL.			
3.	**5.**	**Introduction**: Boolean Algebra: Basic and Axiomatic Definition of Boolean Algebra; Two-Valued Boolean Algebra. Basic Theorems and Properties of Boolean Algebra.	2-1, 2-2, 2-3 &2-4	2-2 Ref Book (3)	
	6.	Boolean Functions; Canonical and Standard Forms.	2.5 &2-6		
	Lab 03	Derivation of Boolean Functions from given logic diagram and its Hardware implementation. Function implementation using Verilog HDL Gate-Level modeling.			
4.	7.	Other Logic Operations. Digital Logic Gates and Integrated Circuits.	2-7, 2-8, & 2-9	8-1 Ref Book (5)	
	8.	Problem Solving Session			
	Lab 04	Minimization of Boolean Functions and its Hardware implementation.			
5.	**9.**	**Introduction**: The K-Map Method; Two and Three -Variable K- Maps. Sum-of-Products (SOP) simplification using Three-Variable K-Map. Sum-of-Products (SOP) simplification using Four-Variable K-Map; Essential and Non-essential Prime Implicants.	3-1, 3-2, & 3-3	5-2 Ref Book (4) 5-3 Ref Book (4) 2.5 Ref Book (3)	
	10.	Five-Variable K-Map; Sum-of-Products (SOP) simplification using Map Method, Product- of- Sums (POS) Simplifications and Don't Care conditions.	3-4, 3-5 & 3-6	5-4 Ref Book (4)	
	Lab 05	Design of Binary-to-Gray/Gray-to-Binary Code Converter using basic gates. Gate-Level Modeling of Combinational Circuits using Verilog HDL.			
	11.	Quine-McCluskey Minimization algorithm (Tabulation).		6-1, 6-2 &6.3 Ref Book (4)	
	12.	NAND and NOR implementations.	3-7		
	Lab 06	BCD-to-Seven Segment Decoder Design.			
7.	13.	Other Two-Level implementations. Exclusive-OR function: Parity Generation and Checking.	3-8, & 3-9		

	14.	**Introduction**: Combinational Circuits: Design Procedure with Code Conversion Example.	4-1, 4-2 & 4-4		
	Lab 07	Design of a 2-bit Magnitude Comparator using Classical design method. Combinational Logic Design using Verilog HDL.			
8.	15.	Combinational Circuits: Analysis Procedure. Half and Full Adders	4-3, & 4-4		
	16.	Design of 4-BIT Ripple Carry and Carry Look-ahead Adder-Subtractor using Full Adders, Overflow	4-5		
	Lab 08	Design of a 2-bit Adder/Subtractor Circuit. Combinational Logic Design using Verilog HDL.			
9.	**Mid Semester Exam**				
10.	17.	Decimal Adder, Binary Multiplier	4-6, & 4-7		
	18.	Magnitude Comparator, Decoders/De-multiplexers	4.8, & 4-9		
	Lab 09	Design of 4-bit ALU.			
11.	19.	Encoders.	4-10	4-2-2, 3, &4 Book (6)	
	20.	Multiplexers and Tri-State Gates.	4-11		
	Lab 10	Voting Machine Design.			
12.	**21.**	**Introduction**: Sequential Circuits and different types of Latches.	5-1, 5-2, & 5-3		
	22.	Storage Elements: Flip-Flops, Other Flip-Flops, Conversion of Flip-Flops.	5-4	11-4,11-5,11-6 &11-7 Ref Book (4)	
	Lab 11	Memory Elements: Latches and Flip-flops. Design of a positive-edge triggered D flip-flop.			
13.	23.	Analysis of Clocked-Sequential Circuits; State Equations, State Table, State Diagram, and Flip-Flop input equations.	5-5		
	24.	Analysis with D Flip-Flops, JK Flip-Flops, and T Flip-Flops. Mealy and Moore Models.	5-5		
	Lab 12	Flip-Flop Applications & Proteus Simulation of Digital Circuits			

14.	26.	State Reduction using Row Matching and Implication Table Techniques. State Assignment Method.	5-7	15.3 Ref Book (4)	
	26.	Design Procedure- Synthesis using D Flip-Flops, JK Flip-Flops, and T Flip-Flops.	5-8		
	Lab 13	Sequence Detector Design. Sequential Logic Design using Verilog HDL			
15.	**27.**	**Introduction**: Registers with Parallel Load.	6-1		
	28.	Shift Registers; 4-Bit Shift Register; Serial Transfer and Serial Addition.	6-2		
	Labs revision				
16.	29.	4-Bit Universal Shift Register.	6-2		
	30.	Ripple Counters; Binary and BCD Ripple Counters.	6-3		
	Lab Final Exam				
17.	31.	Synchronous Counters; Binary and BCD Counters.	6-4		
	32.	Other Counters; Counter with unused States. Ring Counter and Johnson Counter	6-5		
18	**End Semester Exam**				

Lab Experiments:	
Lab 1: Familiarization of Basic Gates and Digital ICs	
Lab 2: Introduction to Verilog HDL. Basic language constructs and design entry using Verilog HDL.	
Lab 3: Derivation of Boolean Functions from given logic diagram and its Hardware implementation. Function implementation using Verilog HDL Gate-Level modeling.	
Lab 4: Minimization of Boolean Functions and its Hardware implementation.	
Lab 5: Design of Binary-to-Gray/Gray-to-Binary Code Converter using basic gates. Gate-Level Modeling of Combinational Circuits using Verilog HDL.	
Lab 6: BCD-to-Seven Segment Decoder Design.	

Lab 7: Design of a 2-bit Magnitude Comparator using Classical design method. Combinational Logic Design using Verilog HDL.	
Lab 8: Design of a 2-bit Adder/Subtractor Circuit.Combinational Logic Design using Verilog HDL.	
Lab 9: Design of 4-bit ALU.	
Lab 10: Voting Machine Design.	
Lab 11: Memory Elements: Latches and Flip-flops. Design of a positive-edge triggered D flip-flop. Sequential Logic Design using Verilog HDL	
Lab 12: Flip-Flop Applications & Proteus Simulation of Digital Circuits	
Lab 13: Sequence Detector Design. Sequential Logic Design using Verilog HDL	

Grading Policy:	
Quizzes Policy	The quizzes are a mandatory component of the overall assessment. The purpose of quizzes is to keep the students up-to-date with the lecture material and test basic understanding of the course concepts. There will be at least **6** unannounced quizzes conducted in the class any time during the lecture. Each quiz will consist of questions that target specific topics from the most recent as well as previous week lectures. An additional quiz will be from class participation and evaluation will be based on student's active involvement in different online interactive forums made available to them.
Assignments	In order to give sufficient practice and comprehensive understanding of the subject, a minimum of 4 home assignments will be given to the students. The questions in assignments will be challenging to give students the confidence and enable them to prepare for the exams well. Home works will be submitted at the beginning of class on the due date. The students are advised to do the assignment themselves. Copying of assignment is highly discouraged, taken as cheating case and dealt accordingly. No late submissions will be accepted.
Conduct of Labs	The labs will be conducted for three hours each week. For the conduct of lab, the students will be divided into groups with 2/3 students per group. A lab handout comprising pre-lab, in-lab, and post-lab report parts will be provided to students for study and analysis during the week preceding each lab session. The students are expected to complete pre-lab work before lab starts and also come prepared for the lab. Any student failing to complete pre-lab will not be allowed to attend lab session. The students will be evaluated during each lab on the basis of demonstration, oral viva, and lab report submitted by them individually on completion of lab work. The students are required to be punctual in the lab; late comers will be penalized in award of marks.
Final Lab Exam	The students will be evaluated in the final lab exam as per the schedule shared with the students. Each student will be assessed individually based on oral exam and hardware implementation of any given circuit in the lab. The students are expected to come prepared for the lab exam.
Other Matters:	

Online Discussions	MS Teams link will be created and shared with the student, if the need arises. Besides this, a WhatsApp group will also be created for each section by the respective Class Representatives during first week of semester commencement. This group will be used for course-related assignments/collective queries. Individual clarifications will be addressed separately.

Academic Honesty and Plagiarism

Plagiarism is the unacknowledged use of other's work, including the copying of assignments and laboratory results from the other students. Plagiarism is considered a serious offence by the university and severe penalties apply. Therefore, all the students must display originality of efforts and avoid plagiarism in any form.

Classroom Etiquettes

It is the collective responsibility of all the students to make the class environment conducive for learning. To create and maintain a friendly atmosphere, the following standards of class room behavior will be observed: -

1. Students will be punctual for the class. The teacher considers late comers disrespectful of those who manage to be on time.
2. If a student decides to attend the class, he or she will not disrupt class by leaving before the lecture has ended.
3. All the cell phones must be switched OFF prior to entering the class room.
4. The students must bring text book and calculators in the class and make lecture notes.

A Few Tips for Good Learning and Grade Management

1. Punctuality and active participation in the class activity
2. Apriori study of course material to the taught in the class
3. Timely and non-plagiarized assignment submissions.
4. Regularity in lab work and adherence to lab rules/instructions.
5. Compensation for any missed evaluation immediately after occurrence.
6. Optimal use of online forums created for the students.
7. Problem solving of end chapter problems in the text and reference books
8. Judicious time management during different evaluations like quizzes, labs, and comprehensive exams.
9. Timely selection and prototyping of semester design project and its completion well before the deadline.
10. Effective utilization of office hours i.e academic discussion with teacher
11. Regular monitoring of class and lab attendance and intimate anomaly, if any.

Tools / Software Requirement:

1. Verilog Hardware Description Language (Verilog HDL) software and HDL simulator ModelSim version 5.7f will be used for the design and simulation of logic circuits.
2. Digital and Embedded Systems lab will be used for hands on practice.